Resonance of a Distribution Feeder with a Saturable Core Fault Current Limiter

Christopher R. Clarke *Member*, IEEE, Franco Moriconi, Amandeep Singh, *Member*, IEEE, Ardalan Kamiab, Russ Neal, Alonso Rodriguez, *Member*, IEEE, Francisco De La Rosa, *Senior Member*, IEEE and Nick Koshnick

***Abstract*-- Simulations of a resonance event were performed based on actual field data of a commercially operating distribution feeder and a superconducting saturable core fault current limiter. The analysis was conducted from both the system's and the fault current limiter's perspectives. Agreement in the results of the two approaches showed that under certain values of reactive shunt compensation, full insertion of the limiter's reactance, and low load conditions, a sustained but damped resonance can occur. Resonance suppression preventive measures for these conditions are proposed.**

***Index Terms*— Capacitive energy storage; Fault current limiters; Inductive energy storage; Resonance; Saturable cores; Short circuit currents**

I. Nomenclature

CoF – Circuit of the Future
HTS – High temperature superconductor
FCL – Fault current limiter
LC – Inductive and capacitive circuit
SCE – Southern California Edison
ZP – Zenergy Power, Inc.

II. Introduction

A. Nature of Electrical Resonance

Resonance in a system occurs when a small driving perturbation results in large effects in the system. In an electrical circuit involving inductive and capacitive reactances, the resonance effect can be generated when the absolute values of these two reactances are equal. For a given circuit, this equality will be true only for a particular resonant frequency.

Physically, during electrical resonance, when a charged capacitor is connected across an inductor in an RLC circuit, charge will flow through the inductor's coils. Energy is stored in the inductor's magnetic field and the voltage in the capacitor is reduced until all the charge on the capacitor plates is depleted. However, current flow continues because inductors oppose changes in current, and current is induced by the collapsing magnetic field of the inductor. This current charges the capacitor with a voltage of opposite polarity of the original charge until the magnetic field's energy is dissipated. Current flow stops and the capacitor will again store all the charge and the discharge-charge cycle repeats, but current flows in the opposite direction.

As described, this is generally a highly efficient process, as the only opposition to current flow in the circuit is the resistance of the circuit. In most power circuits the total resistance of the line conductors and other components is relatively small compared to the reactive impedance. Typically, the value of resistance can usually be ignored for most calculations, thus simplifying the circuit to an LC model.

Yet, it is this high circuit efficiency during inadvertent resonance that causes concern. Depending on whether a series or a parallel LC circuit is formed, either high voltages or high currents can be generated. In this case study, the resonant circuit formed was a series circuit, as described in the following sections.

Depending on the circuit's parameters, resonance can develop into serious problems. If damping of the resonance oscillations is not sufficient and the conditions that generated resonance are sustained, energy can accumulate to extremely high levels. In particular, if the magnitudes of the resonant voltages or currents are lower than the normal settings of conventional protection relays; this undetected sustained condition can lead to extreme energy build-up with every input cycle from the system.

B. HTS Fault Current Limiter Demonstration on the 12 kV Distribution Circuit of the Future (CoF)

Southern California Edison's Distribution Field Engineering envisioned, installed and has commissioned a dedicated 12 kV feeder to demonstrate and obtain service experience with state-of-the-art equipment and operating procedures that could result in increased system reliability and lower costs. This feeder is known as the Circuit of the Future (CoF). Zenergy Power's high temperature superconductor fault current limiter (HTS FCL) is installed at the substation feeding the CoF.

The FCL is connected in series between the feeder loads and the 12 kV side of the substation's transformer bank. The purpose of the installation is to demonstrate the limiter's functions and gain operational and maintenance experience under real-world conditions.

The FCL is designed to operate as an inherently variable reactance based on the fact that the FCL's insertion reactance is proportional to the slope of its B-H curve. As illustrated in Fig. 1, under normal operating conditions the FCL has a very low series reactance, but under fault conditions it changes to a very high reactance within a millisecond, in order to limit the current surge to a desired safe level. When the fault is cleared,

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C. R. Clarke, A. Kamiab, and R. Neal are with Southern California Edison, Rosemead, CA, USA.

F. de la Rosa, A. Singh, F. Moriconi, and A. Rodriguez and Nick Koshnick are with Zenergy Power, Inc., South San Francisco, CA, USA.

the operating point automatically returns to its normal state corresponding to a very low series reactance, hence a low voltage drop during steady state.

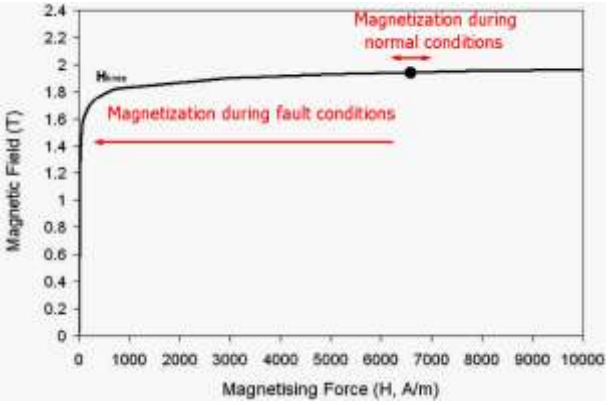

Fig. 1. Operating region of the saturable core FCL.

Fig. 2 shows a single-phase arrangement of the FCL. An HTS coil provides the DC bias to saturate the two cores of every phase. For a three-phase configuration, six core limbs (two per phase) pass through the DC coil.

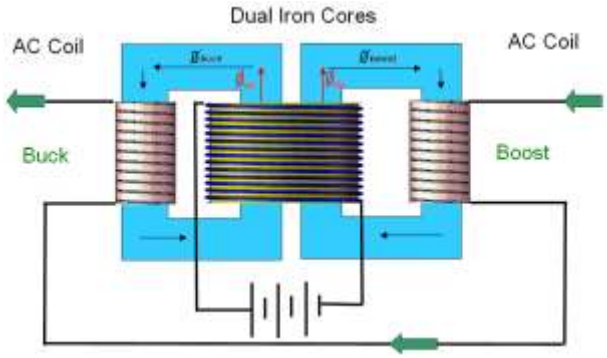

Fig. 2. Dual iron cores saturated by an HTS DC coil in a single-phase FCL.

III. RESONANCE EVENT DESCRIPTION

A. State of the Circuit

1) Feeder Elements:

The CoF is a 12kV distribution feeder serving approximately 1,500 mostly residential customers in San Bernardino County, California. The mainline or 'backbone' of the circuit is approximately 8.5 miles long, and is comprised of 25% overhead construction and 75% underground construction.

The saturable-core fault current limiter (FCL) is installed inside the substation fence line immediately beyond the main feeder circuit breaker (CB 0 in Fig.3). The FCL is also equipped with a bypass switch.

There are four shunt capacitor banks installed on the CoF for VAR and voltage support. At the time of the event two of the four capacitor banks were disabled. The remaining in-service capacitor banks are rated at 1.2 MVAR and a 1.8 MVAR. Both banks are connected wye ungrounded and are capable of switching automatically. Prior to the event the 1.8 MVAR bank was closed, and the 1.2 MVAR bank was open.

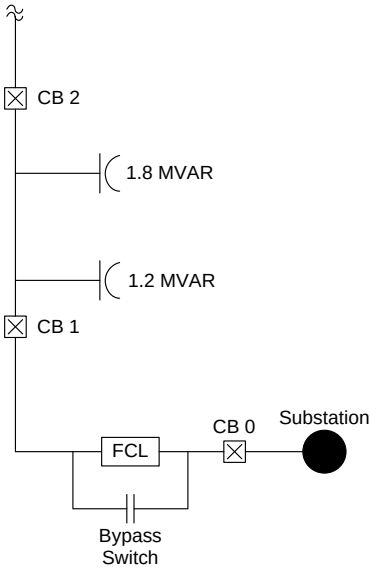

Fig. 3. Diagram of the CoF relevant to the resonance event.

The switchable capacitor banks operate on a time-biased voltage control. The switched capacitor banks open or close if the voltage is measured outside of a programmed dead-band for a set duration. The capacitor banks also are set to perform an emergency open or close if the voltage is measured at 130 V or 110 V (on a 120 V base) respectively for five seconds. The 1.8 MVAR capacitor bank is programmed to open on 124.5V and close on 120.0V (on a 120V secondary base voltage), and has a delay of 60 seconds. The 1.2 MVAR bank was programmed to open on 125.0V and close at 121.0V (on a 120V secondary base voltage) and has a delay of 180 seconds. It is important to note that the capacitor controls are set with a five minute delay before a capacitor bank can perform another open or close operation. Data was sampled at CB 1 and CB 2 where SEL-351 relays from the CoF's advanced protection scheme were monitoring and reporting A-B phase voltage, and phase current every 5 seconds.

2) FCL Status Before Resonance

Prior to DC bias current loss on March 16, 2009, the FCL was operating normally. The FCL's inductance is not a unique number even during normal operating conditions, but is a function of instantaneous AC current. The equivalent inductance of the FCL is shown in Fig. 4.

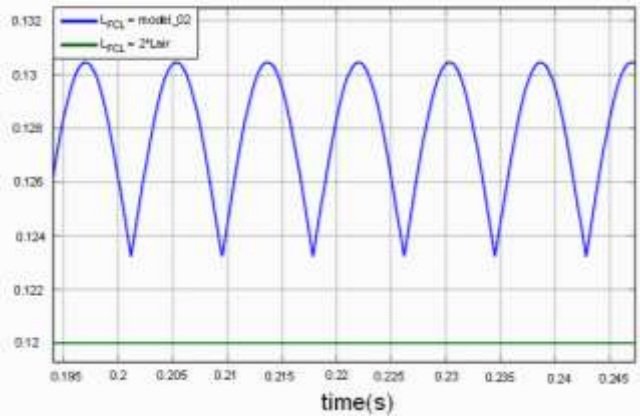

Fig.4. Equivalent FCL inductance (mH) at 100 A DC and 120 A rms.

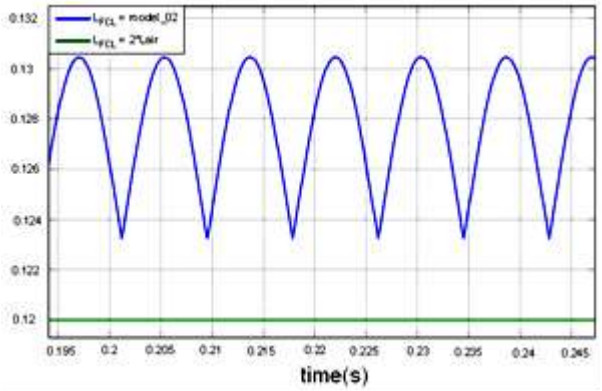

Fig. 5 shows the simulation of the FCL's induced emf at 8 volts peak.

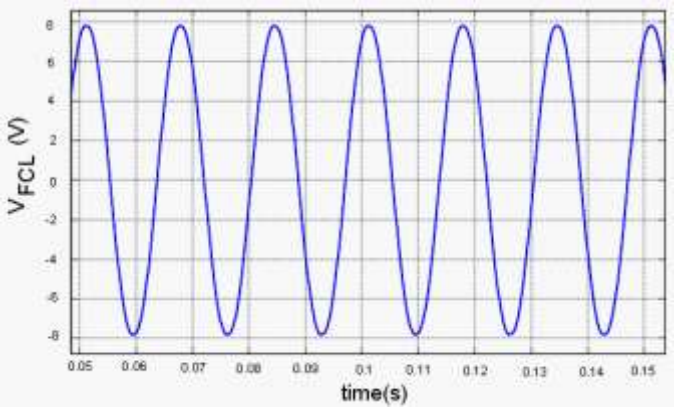

Fig.5. FCL emf in normal mode with 120A AC.

An FFT analysis of the FCL voltage revealed a very clean waveform with less than around 3% of the third harmonic.

B. Resonance Sequence of Events

1) Onset:

As shown in Fig. 6, at 10:10am the DC bias current source shut off initiating the feeder's voltage rise.

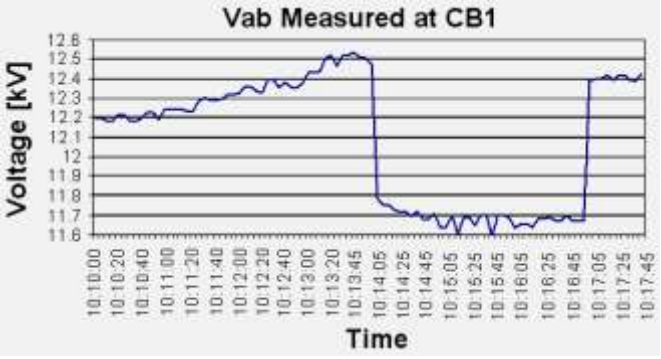

Fig.6. Line-to-line voltage between A and B phases at CB 1 for the first 18 minutes of the event.

Current in the DC coil took approximately 5 minutes to decay to trace levels. Fig. 7 shows the HTS coil's DC current (blue) and its voltage (red) during the event. The coil voltage dropped from predominantly resistive 120mV to predominantly inductive -2 V, and decayed after several minutes as the HTS current settled to zero.

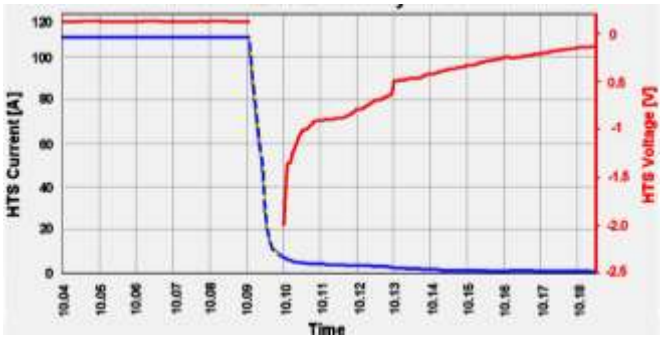

Fig.7. HTS coil current (blue) and voltage during the event.

At 10:13am, three minutes into the event, the system voltage had risen above the 1.8 MVAR capacitor bank's upper dead-band limit (12.45 kV). After 60 seconds above the dead-band limit, the 1.8 MVAR capacitor opened. Without a capacitor bank, the system voltage dropped to about 11.65kV at 10:14am. At approximately 10:17am the 1.2 MVAR capacitor bank switched in due to the system voltage being below the dead-band lower limit for three minutes. This action caused the feeder to re-enter a resonance condition. As a result the voltage increased to 12.4kV. The feeder voltage remained at 12.4 kV until the FCL was manually bypassed at approximately 11:35am, as depicted in Fig. 8. A loud humming sound in the FCL was due to the high magnetostriction of the iron cores undergoing large flux variations. After the FCL was bypassed, the system voltage dropped to approximately 12.2kV, which was approximately the same voltage as before the event.

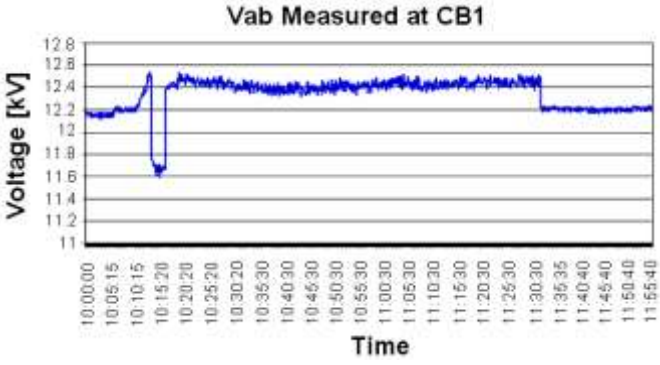

Fig.8. Line-to-line voltage between A and B phase at CB 1 from 10 minutes before the event to 25 minutes past the end of the event.

Fig. 9 shows the line-to-line voltages, as measured by the three potential transformers installed at the load side of the FCL. HTS current (red) also appears for reference. Both feeder voltage and feeder current as measured at the FCL agreed with SCE's field data.

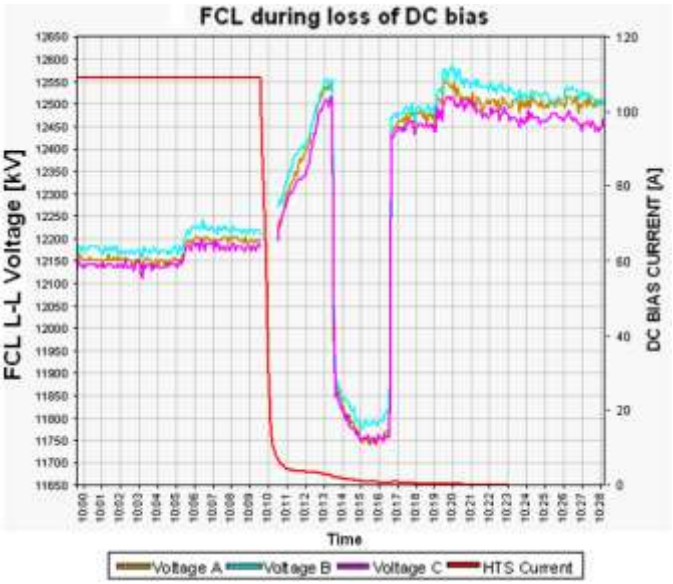

Fig. 9 Three-phase RMS line voltages.

2) Resonance Observed:

The measured voltage resulted from the combination of two opposite effects. The bus voltage increased due to resonance with the 1.8 MVAR capacitor, while the bus voltage decreased due to the voltage drop across the de-saturating FCL. When the event occurred, resonance effects out-weighed the FCL's voltage-drop. A net voltage increase on the bus was measured.

Note that the 1.8 MVAR capacitor bank switched out before the DC coil's current decayed to trace amounts. If the DC coil had decayed to trace amounts before the 1.8 MVAR capacitor bank opened, simulations show the line voltage would have risen to 12.65kV. Under normal system conditions, simulations show the voltage rise due to the 1.8 MVAR and the 1.2 MVAR capacitor banks would be about 0.2 kV and 0.12 kV, respectively.

When the 1.8 MVAR bank opened, the resonance condition ceased and the system voltage dropped to 11.87kV. This voltage drop from 12.2 kV was due to the FCL's voltage-drop under de-saturating conditions. This measurement allows comparison of the line-voltage for the saturated FCL with respect to that for the de-saturating FCL without a masking effect due to resonance. The line voltage decrement from 12.2 kV (saturated FCL) to 11.87 kV was caused by the FCL's voltage drop. Furthermore, the DC current was still decreasing causing the FCL's voltage drop to increase, resulting in a further decrease to 11.65 kV.

IV. Resonance Analysis

A. *Analysis from the Circuit Perspective*

1) Relative Inductance and Capacitance Values

The impedance of a single phase of a 1.2 MVAR capacitor bank is 129.6 Ω, and 86.4 Ω for a 1.8 MVAR capacitor bank. Due to the non-linear nature of the FCL, an rms value was used. During the event, a maximum rms inductance of 0.020 H, or 7.5 Ω was measured. The maximum instantaneous inductance value calculated during simulation was 0.030 H. Maximum resonance occurs when inductance and capacitance are equal. During the event, the capacitor banks would have needed to be more than ten times larger to cause a worst case resonance condition. Figures 10-12 show the PSCAD simulation results describing instantaneous inductance, rms inductance and harmonic orders, respectively. Observe in Fig. 12 that without any capacitor banks in series, the resonant frequency rises to a very high order number beyond the graph's scale boundary.

Also note that the PSCAD charts have an accelerated time scale due to the lengthy processing time to run the EMTDC algorithm. At 4 seconds the 1.8 MVAR capacitor bank opens, at 7.5 seconds the 1.2 MVAR capacitor bank closes, and at 15.5 seconds the FCL is bypassed.

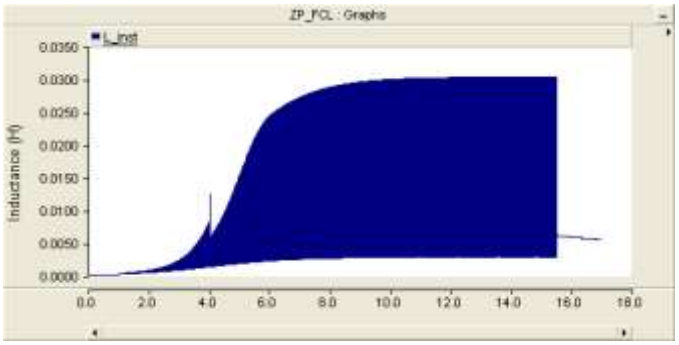

Fig. 10. FCL instantaneous inductance.

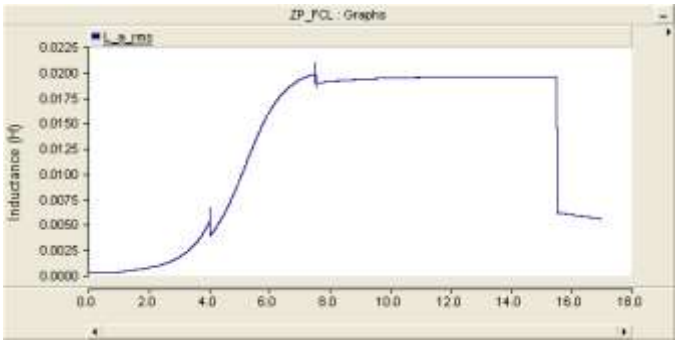

Fig. 11. FCL rms inductance.

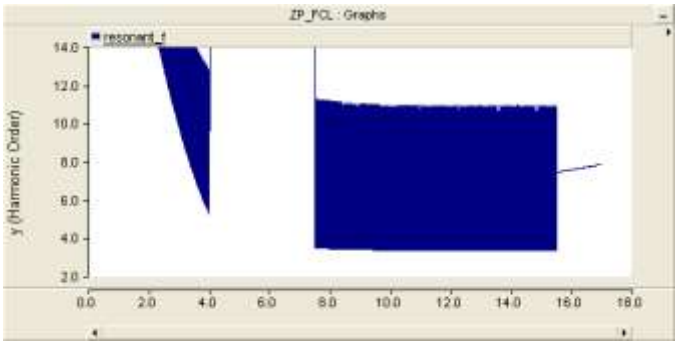

Fig. 12. FCL harmonic numbers. Note the time scale was accelerated in PSCAD modeling.

2) Load Magnitude Levels

Prior to the event the feeder was loaded at approximately 120A per phase. As a series resonance causes an increase in voltage and not current, load levels remained relatively constant until the 1.8 MVAR capacitor bank opened.

Due to SCE's distribution design practice of using shunt capacitor banks for VAR supply and voltage support, the power factor was leading at the time of the event. Just before the 1.8 MVAR capacitor bank opened, about 1.1 MVAR was flowing through CB 0 back to the source. When the 1.8 MVAR capacitor bank opened, 0.5 MVAR VARs was supplied by the substation source, causing the load to drop by a net 0.6 MVAR, about 25A.

When the 1.2 MVAR bank closed, an excess of reactive power was supplied by the 1.2 MVAR bank and the current increased by approximately 12A. Figures 13 and 14 describe the calculated MVAR demand on the load side of CB 0 and the load side of the FCL, respectively. Figure 15 illustrates the measured phase current on phase A.

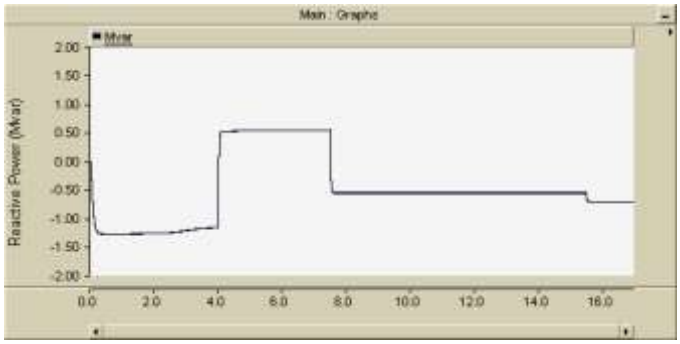

Fig. 13. Simulated MVAR demand at CB 0.

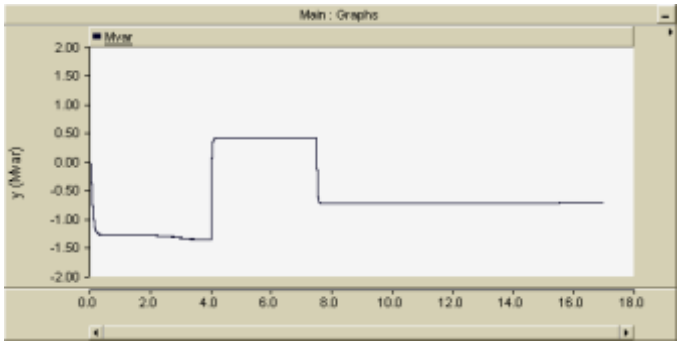

Fig. 14. Simulated MVAR demand downstream of the FCL.

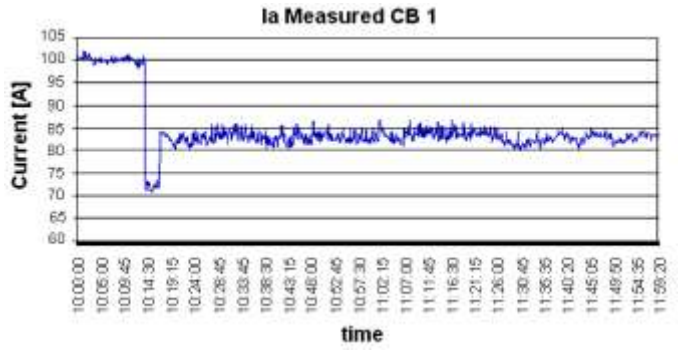

Fig. 15. Ia measured at CB 1. Note there are about 20A of load between CB 0 and CB 1.

B. Analysis from the Fault Current Limiter Perspective

1) Simulations of Normal Operating Conditions

The induced emf across each phase of the FCL is a function of DC bias and AC load currents. It can be represented by the following function:

$$emf(i_{ac}) = -n_{ac}A_{core}\frac{\partial B}{\partial i_{ac}}\frac{\partial i}{\partial t} = -n_{ac}A_{core}\Im(i_{ac}, B_{sat}, I_{\max}, K)\frac{\partial i}{\partial t} \quad --(1)$$

$$-I_{\max} \le i_{ac} \le I_{\max}$$

$$emf(i_{ac}) = -Lair\frac{\partial i}{\partial t} \quad --(2)$$

$$|i_{ac}| \ge I_{\max}$$

Where:
n_{ac} is the number of AC turns per coil,
A_{core} is the core cross section contained by the AC coil,
i_{ac} is the instantaneous line current,
B_{sat} is the magnetic flux density in the core material at saturation. The derivative of B with respect to i_{ac} is a function of geometry, DC bias current, and AC load current.
I_{max} is the maximum AC peak current needed to fully de-saturate the cores,
K accounts for the level of DC bias current,
L_{air} is the equivalent air-core inductance of a single AC coil,
$\Im$ is the FCL function.

A simplified PSCAD circuit was used, as shown in Fig. 16, to test the FCL model under normal conditions.

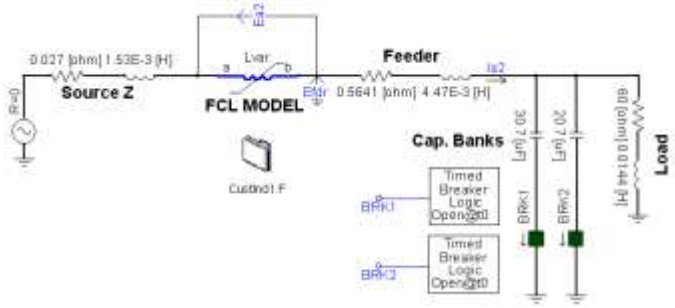

Fig. 16. Simplified PSCAD model of CoF FCL.

The results of the simulations for normal operation conditions appear in Section III.A.2.

2) Simulations of DC Current Loss Conditions

The PSCAD model in Fig. 16 was adapted to simulate the DC bias current loss and the resonance phenomenon. The results closely simulate the actual DC bias current decay as shown by the black curve in Fig. 17. The event was simulated by estimating the transient decay of the DC bias current and calculating the transient increase of the FCL inductance. This can be compared with Fig. 7 which shows measured DC current decay.

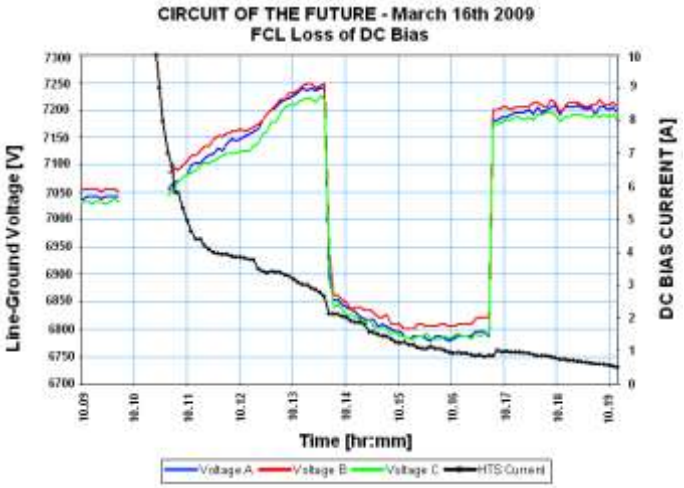

Fig. 17. DC bias current loss and line voltage dynamics.

Fig. 18 shows the simulation of the FCL voltage over a period of several minutes. The voltage increased steadily over that period, reaching a peak value of 700V at the time of complete loss of DC bias current.

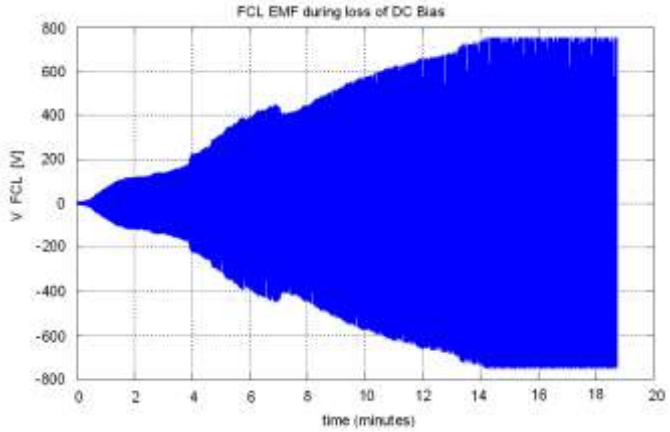

Fig.18. FCL emf during the loss of DC bias current event.

Fig. 19 shows the rms value of the FCL voltage drop. At the end of the DC bias current decay, the maximum FCL voltage drop was of the order of 400V rms.

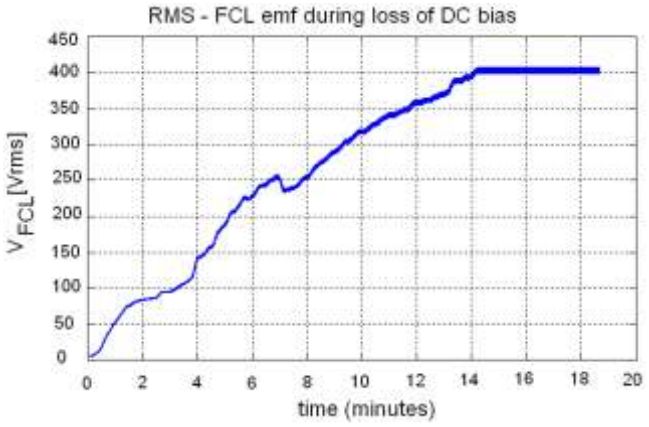

Fig.19. rms FCL emf during loss of DC bias current event.

An FFT of the computed bus voltage was simultaneously performed. As the FCL model transitioned deeper into de-saturation; the 3rd, 5th, 7th & 9th harmonics started to appear in succession as illustrated in Fig. 20. The fundamental frequency component showed a substantial increase from 6V under saturated conditions, to about 800V under loss of DC bias current.

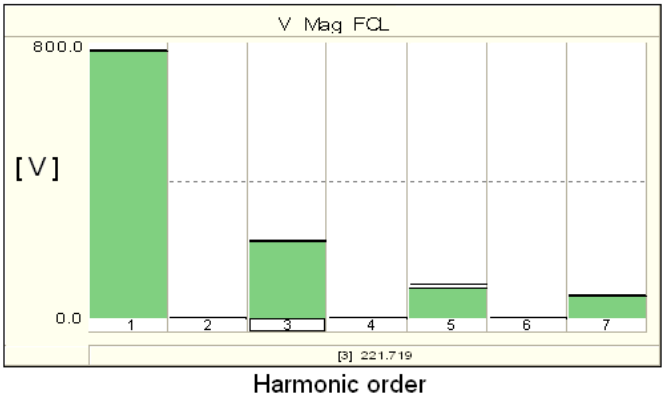

Fig. 20. FFT of FCL voltage with harmonic content

Fig. 21 shows the simulated transient dynamics of the equivalent FCL inductance during this period. As the DC current decreased exponentially, the instantaneous AC current was able to alternately swing the cores more and more into de-saturation and saturation. This was reflected in terms of larger swings in the instantaneous values of inductance riding upon an almost linear increase in inductance as shown in Fig. 21. This also relates with the observed increase of the fundamental component of the FCL's emf during the event, which in turn produced a linear increase in the line voltage (color traces in Fig. 17).

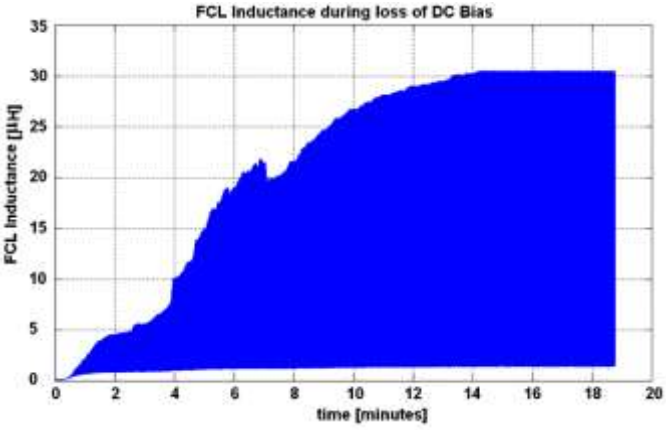

Fig.21. Instantaneous FCL Inductance during loss of DC bias current event.

3) Simulations of Increased Load Current

A series of simulations with increasing AC load current, keeping everything else constant, were analyzed to determine if there was a certain load current value that would yield a voltage rise due to resonance equal and opposite to the FCL's

voltage drop. It was found that at a load current of approximately 250A, the two effects were equal and opposite, and bus voltage no longer increased despite a DC bias current loss condition. See Fig. 22 for simulated bus voltage at 250A load current.

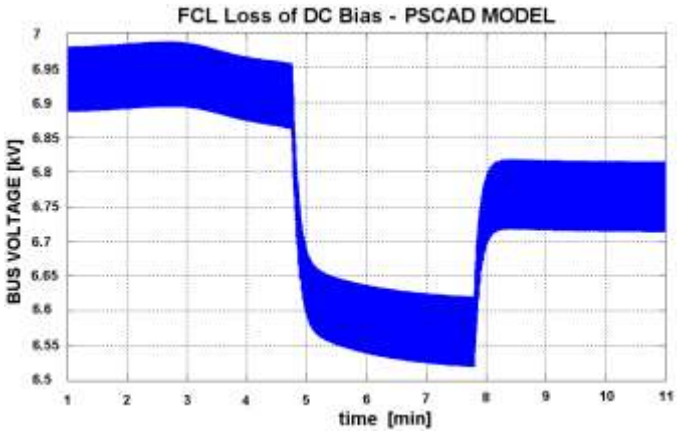

Fig. 22. Simulated bus voltage with AC load of 250A (includes DC current decay).

For AC loads exceeding 250A, the FCL voltage drop always out weighed the resonance voltage effects and the bus voltage decreased when simulating the loss of DC bias current. Fig. 23 depicts the bus voltage drop at 700A load current.

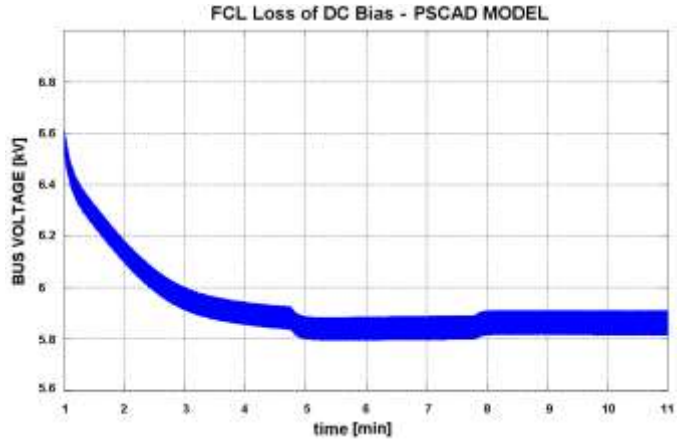

Fig. 23. Simulated bus voltage with AC load of 700 A(includes DC current decay).

V. CONCLUSIONS

A. *Operation Under Low AC Current*

It was confirmed that the Zenergy Power FCL model is capable of closely reproducing the loss of DC bias current event and the resonance condition that followed, as illustrated in Fig. 24.

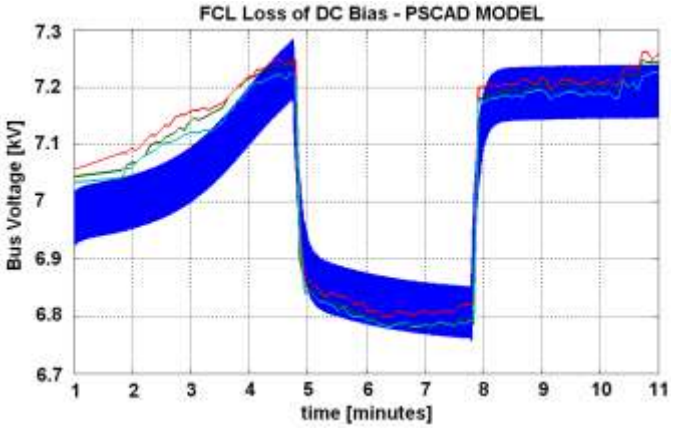

Fig.24. Simulated (blue trace) vs. measured line-to-ground voltage.

It was shown that the instantaneous FCL inductance shows increasing swings riding upon a quasi-exponential rise in inductance as the FCL's DC bias current collapses (see Fig. 18). The steady increase in inductance occurs as the FCL current swings over increasing inductance slopes in the magnetization curve. The protuberance on the FCL inductance in Figs. 18-19 is caused by the increased third harmonic component that develops as the magnetic core loses the DC bias current.

This phenomenon causes an increase in the FCL's rms voltage. This in turn sums with the source voltage, yielding the increased line voltage observed in Fig. 17 and identified here as a resonant condition.

B. *Operation Under Increased AC Current*

It was found that at 250 A of load current, the voltage rise due to resonance was exactly equal in magnitude and of opposite polarity to the FCL's voltage drop, and the bus voltage no longer increased. At load currents in excess of 250 A the line voltage always decreased when simulating loss of DC bias current.

VI. RECOMMENDATIONS FOR RESONANCE SUPPRESSION

A. *Design*

In the design process simulate resonance, including capacitor banks in the line where the FCL is to be installed at different loading conditions, to check for extraordinary events in the controller's logic. This entails an increased FCL inductance under de-saturation condition.

B. *Operational*

The ideal protection against resonance in this case is to immediately bypass the FCL. Given that the event evolves relatively slowly, an automated switch that can operate on the order of seconds is adequate.

Fixed capacitor banks should be avoided. This measure is recommended, because if the automated bypass switch would fail to close, the capacitor banks could be disconnected automatically.

Lastly, base loading of the circuit should be increased, if operating conditions allow this.

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BIOGRAPHIES

Christopher Clarke joined Southern California Edison in April 2004. His primary experience at SCE includes distribution analysis, distribution planning, and power systems modeling. He earned a Bachelor of Science degree in Electrical Engineering from the University of California at Los Angeles, and is pursuing a Master of Science degree in Electrical Engineering at the University of Southern California. He is a registered professional engineer in the State of California and a member of the IEEE.

Franco Moriconi leads Zenergy's engineering effort in the development of a commercial superconducting fault current limiter. Under his technical leadership Zenergy installed and energized its first-ever HTS FCL in the US electric grid. He has being practicing engineering since 1992, when he first joined ABB Corporate Research, actively leading R&D work in the areas of numerical methods and FE simulations, short-circuit strength and noise reduction of power transformers, GIS switchgear technology, and high-speed electrical motors and generators. He participated in two IEC working groups, and was the Convener of the IEC Scientific Committee 17C on seismic qualification of gas insulated switchgear. Currently, he is an active member of the IEEE Task Force on FCL Testing. He earned a Bachelor of Science degree and a Master of Science degree in Mechanical Engineering from UC Berkeley. He is the co-author of six patents in the field of HV and MV electrical machines.

Amandeep Singh has been with Zenergy Power Inc. since January 2008. He holds a Bachelor of Electronics & Telecommunications degree from GNEC, Ludhiana (Punjab). He has worked for ten years in utility generation, transmission and distribution sectors for plant control systems, sub-station O&M and distribution system planning, augmentation, metering and revenue handling. He has an EIT in the State of California and is pursuing a professional engineer's registration. He is a member of IEEE.

Ardalan Kamiab Earned a B.S. E.E. degree at California State Polytechnic, Pomona, CA, and a Project Manager Professional Certification from the University of California Irvine. He is presently Project Manager of the "Smart Grid System of the Future" at Southern California Edison (SCE). Previously he was Project Manager responsible for implementing the design, construction, and operation of the "Circuit of the Future" at SCE. He has also specialized in the area of power quality related to Customer facilities. As an SCE Senior Field Engineer, Ardalan was lead for Distribution Substation Annual Load Planning for two key zones of the SCE system. He also has extensive experience in substation automation utilizing state of the art electronic relaying and communication schemes in both distribution and hydro generation systems. He is a registered professional engineer and a member of IEEE Power Engineering Society: Distribution Automation and Intelligent Grid.

Russ Neal is a Strategic Program Manager for Southern California Edison, specializing in Smart Grid with an emphasis on distribution. Mr. Neal holds a BSEE from the US Naval Academy, an MEEE from the University of Idaho, and an MBA from Azusa Pacific University. He is a registered Professional Engineer in both Electrical and Nuclear Engineering in the State of California. His previous experience includes five years as an officer in the surface nuclear Navy, seventeen years at Southern California Edison's San Onofre Nuclear Generating Station, and twelve years in the Transmission and Distribution Business Unit including service in distribution apparatus engineering, as a district superintendent, and as Manager of Distribution System Engineering.

Alonso Rodriguez has worked thirty-nine years in the electrical power industry in the U.S and Mexico. This experience includes: system planning, operation, and maintenance of public and private generation and power delivery systems; project management; applied research and development; commercialization of utility products; manufacturing quality control; nuclear power plant quality assurance; and fourteen years as graduate power engineering instructor at the University of Southern California. He earned a PhD in Electrical Power engineering from the University of Southern California. Currently he holds a faculty visiting associate appointment in Engineering and Applied Science at the California Institute of Technology. He is a member of IEEE.

Francisco De La Rosa joined Zenergy Power, Inc. in April 2008 at the time the Company was embarked in the development of the first HTS FCL prototype that would become a utility tested unit. He has held various positions in R&D, consultancy and training in the electric power industry for around 30 years. His fields of interest include the smart grid concept, applications of superconductivity in power systems, power quality, and power system protection in utilities and industry. Francisco holds a PhD degree from Uppsala University, Sweden. He is a Collective Member of CIGRE and a Senior Member of IEEE PES where he contributes in several Working Groups.

Nick Koshnick is a consulting engineer with Zenergy Power with expertise in electrical and electromagnetic modeling and superconductivity. He earned a PhD in applied Physics from Stanford University in early 2009.