Integrated Power Management for Active RFID

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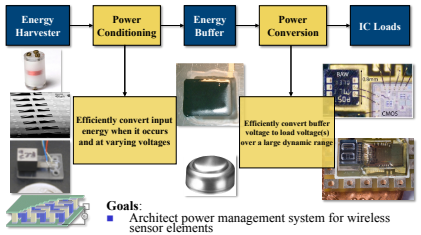
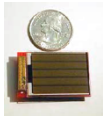
Node Powertrain Structure

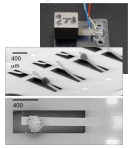


Goals:
- Architect power management system for wireless sensor elements
- Design strategies for power conversion from various energy sources to the energy storage device
- Design of integrated power management interfaces for sensor node subsystem loads.

Energy Harvester Interface Challenges

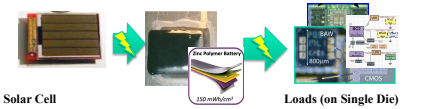
- **Solar Cell**
  - Outdoor: 15000 µW/cm²
  - Indoor: 30 µW/cm²
  - Single cell ~ 0.6V_{oc}
  - MPPT-> optimum energy extraction
- **Thermoelectric**
  - Low V_{oc} 100mV/K
  - 10 µW/K/cm²
  - Power changes w/ temp gradient
- **Piezoelectric**
  - device resonance tuned to anticipated source frequency
  - AC output varies with vibration amplitude
  - 300 µW/cm³



Active RFID Tag

- **Self-powered Active RFID Tag**
  - 10m communication (much further than passive RFID)
  - *50 µW* Wake-up RX Radio and 1mW TX
  - *Self-contained* (postage stamp footprint but only mm's thick)
  - *Fully integrated* IC (single die)
  - *Small solar cell* harvests enough energy for 24 hour operation

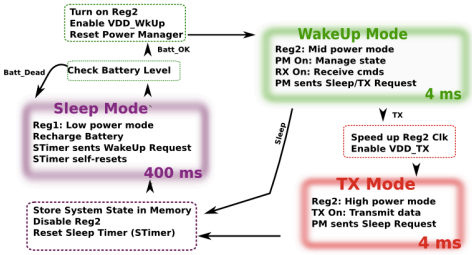


Solar Cell
- 2cmx1cm
- 10µW avg (Indoor)
- V_{oc} = 2.4V, I_{sc}=10uA

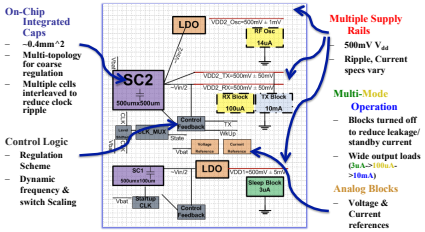
Printed Battery
- 1cmx1cm
- V_{bat} ~ 1.1-1.9V
- Integration w/ substrate

Loads (on Single Die)
- 50 µW RX
- 1mW TX
- 0.5V Logic
- Power Management

Multi-mode Operation



Battery to Load Interface



On-Chip Integrated Caps
- ~0.4mm^2
- Multi-topology for coarse regulation
- Multiple cells interleaved to reduce clock ripple

Control Logic
- Regulation Scheme
- Dynamic frequency & switch Scaling

Multiple Supply Rails
- 500mV V_{dd}
- Ripple, Current specs vary

Multi-Mode Operation
- Blocks turned off to reduce leakage/ standby current
- Wide output loads (3uA->10mA->10mA)

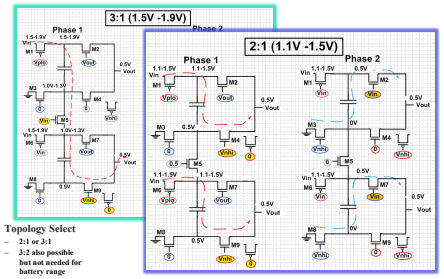
Analog Blocks
- Voltage & Current references
- Low-dropout regulator for finer regulation

Load Power Requirements

Rail	SC Clk	State (WkUp, TX)	Peak/Avg Load	Max Time	Ripple (mV)	Cl	Eng (uC)
Vdd1	100kHz	(X,X)	4uA	.4s	5mV		1.6
Vdd2_Osc	400kHz	(1,0)	15.5/13.5 uA	4ms	1mV	20fF	0.06
Vdd2_RX	400kHz	(1,0)	120/100 uA	4ms	50mV	10pF	0.4
Vdd2_TX	20Mhz	(1,1)	8.5/7mA	10ms	50mV	20pF	70

- Multiple voltage rails needed
- Wide current load range 4uA->8mA (3 orders of magnitude)
- Wake-up RX and heavily duty-cycled TX
  - Reduces Eng/cycle for TX from 70uC to .7uC (1%) or .07uC (.1%)
- Standby mode consumes the most energy per cycle
  - Reduce leakage in standby mode by power gating other rails

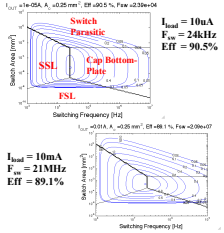
Switched Cap Topology



Topology Select
- 2:1 or 3:1
- 3:2 also possible but not needed for battery range

Switched Cap Optimization

- Cap area, switching freq, and switch area need to be optimized
  - Highly iterative process but can simplify system-level optimizations using circuit-theory based dynamic model (*M. Seeman, 2007*)
- 2 to 1V Conversion Ex.
  - CMOS 65nm process
  - Cap area: **0.25** mm^2
- Losses:
  - SSL (main caps)
  - FSL (conduction)
  - Gate cap
  - Cap Bottom plate
  - Junction cap
- Adjust for efficiency
  - Frequency scaling
  - Switch scaling



I_{load} = 10uA
F_{sw} = 24kHz
Eff = 90.5%

I_{load} = 10mA
F_{sw} = 21MHz
Eff = 89.1%

Future Work

- Efficiency improvements at lower power states (sub uW)
- Wider input voltage range (100mV->10V)
- More/finer conversion ratios
- Regulation over wide output load

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