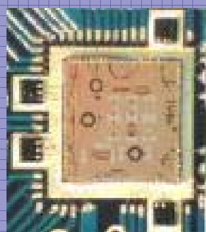
Wireless Sensor Networks

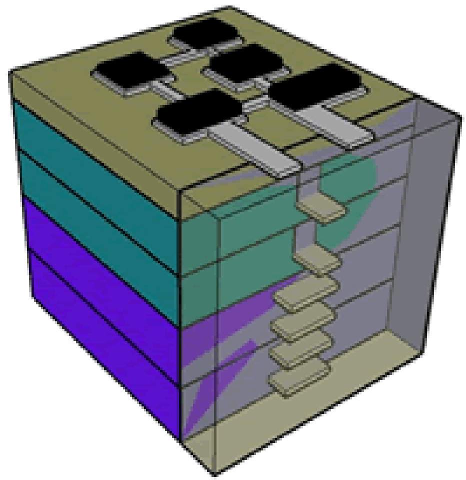
Low Power Radio



“Disappearing Computer”

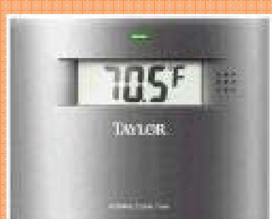
B. Gates, *Economist* (2003)

Energy Storage



“Picocube”

Sensor



Renewable Power

Supply

Micro-Power/Cost Wireless

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Prof. Jan Rabaey

Berkeley Wireless Research Center
UC-Berkeley Dept of EECS

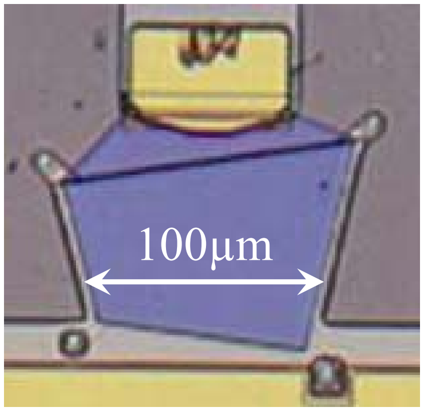
DR-ETD
19 Feb 2008

Micro-Power/Cost Wireless

- Advances in microfabrication and electronic devices create new opportunities for circuit designers
- Unique characteristics of DR application drive new radio architectures
- Combination of advanced devices and new radio architectures delivers wireless communication with very low power and cost

RF-MEMS

Avago FBAR (BAW)



Provides high accuracy frequency reference or high Q filtering

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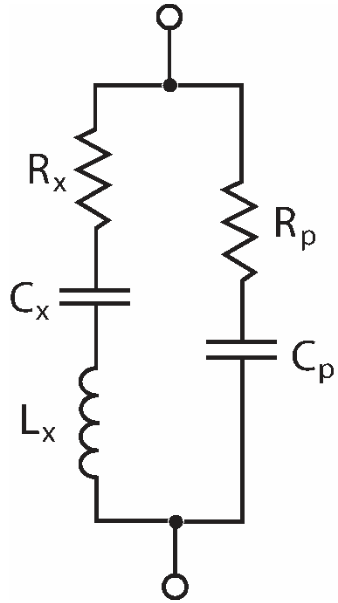
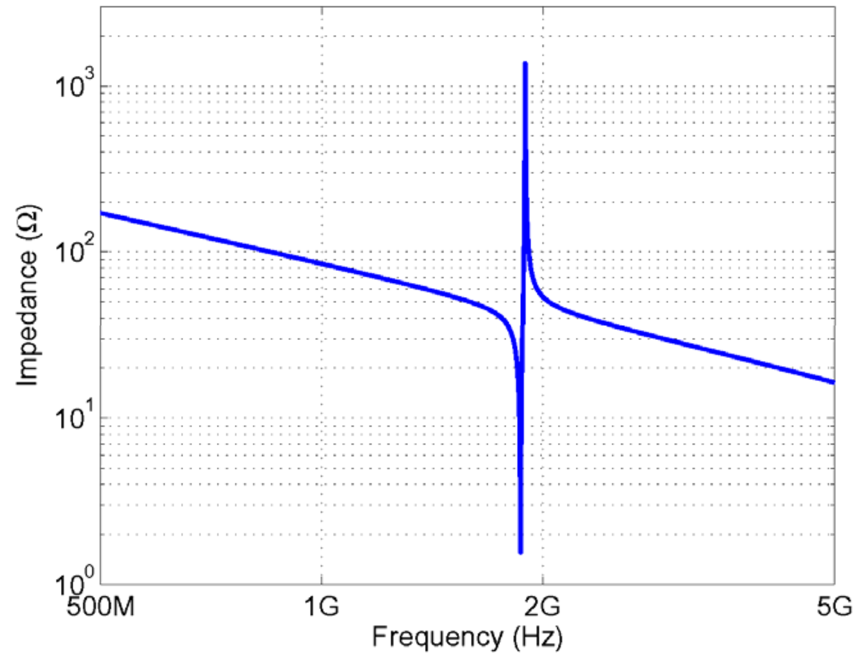


Simulated FBAR impedance response

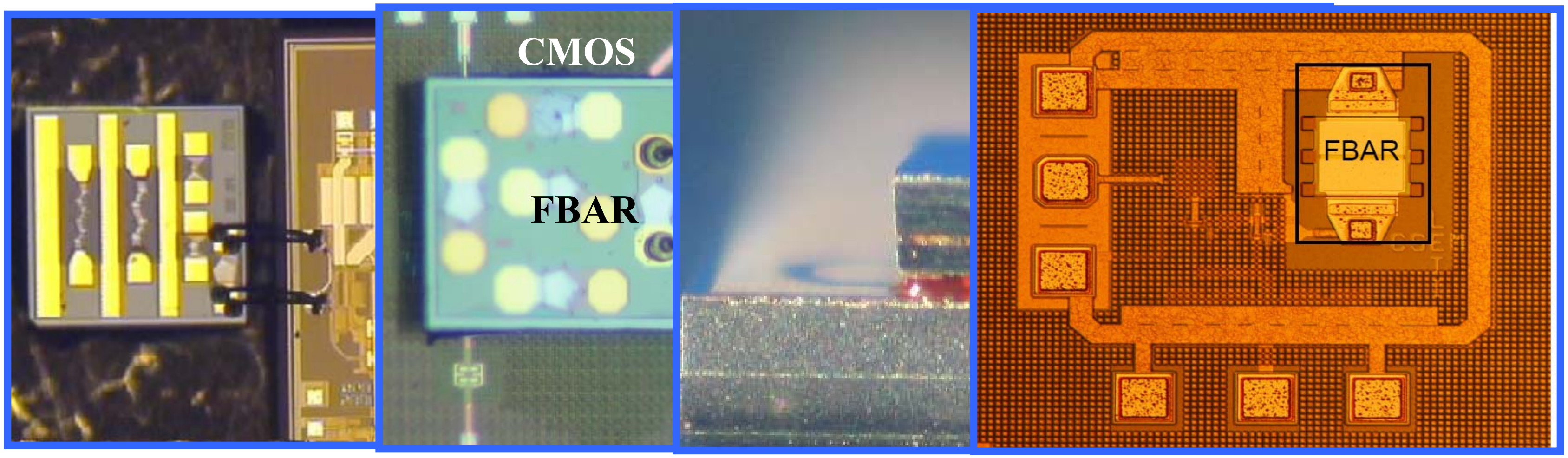


MEMS can replace traditional external components (like crystals) for highly integrated transceivers:

- Reduction in implementation size/volume
- Cost reduction

FBAR - CMOS Integration

- **Many different ways of connecting CMOS with FBAR:**
  - Chip-on-board: mainly for prototyping circuits
  - Chip-on-chip: alternative for small footprint
  - Flip-chip: mature packaging technology
  - Above-IC integration: elegant but expensive

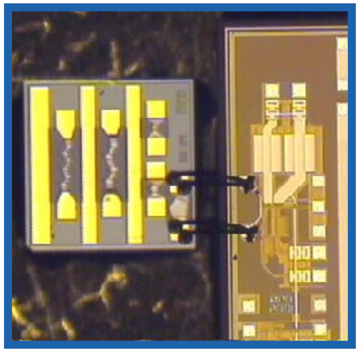


(pictures courtesy by B. Otis, M. Mark)

M. Aissi et al., ISSCC'06

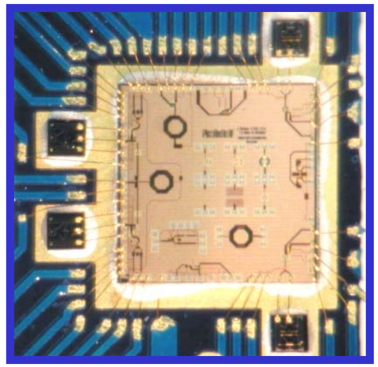
Radio History in the Group

FBAR-based
low power oscillator



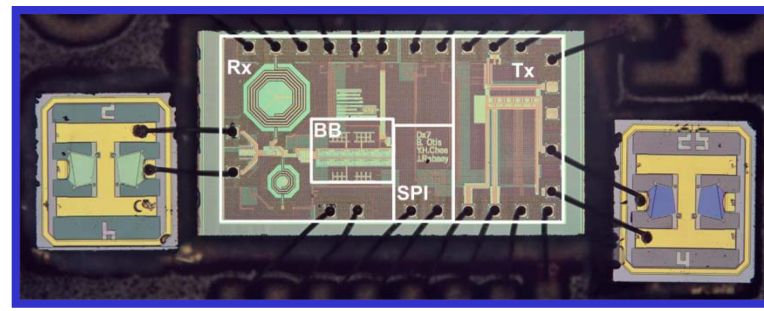
ESSCIRC 2002 (Otis)

2-Channel Prototype Transceiver



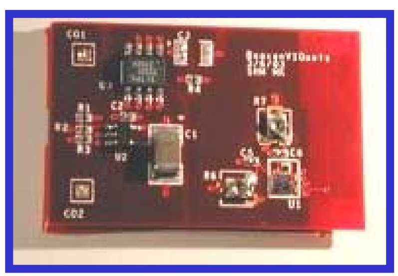
VLSI 2004 (Otis et al)

Super-Regenerative Transceiver



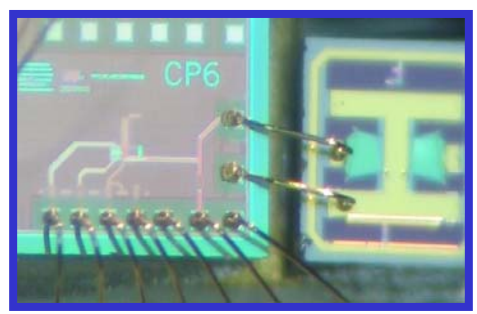
ISSCC 2005 (Otis /Chee)

ISPLED 2003 (Roundy et al)



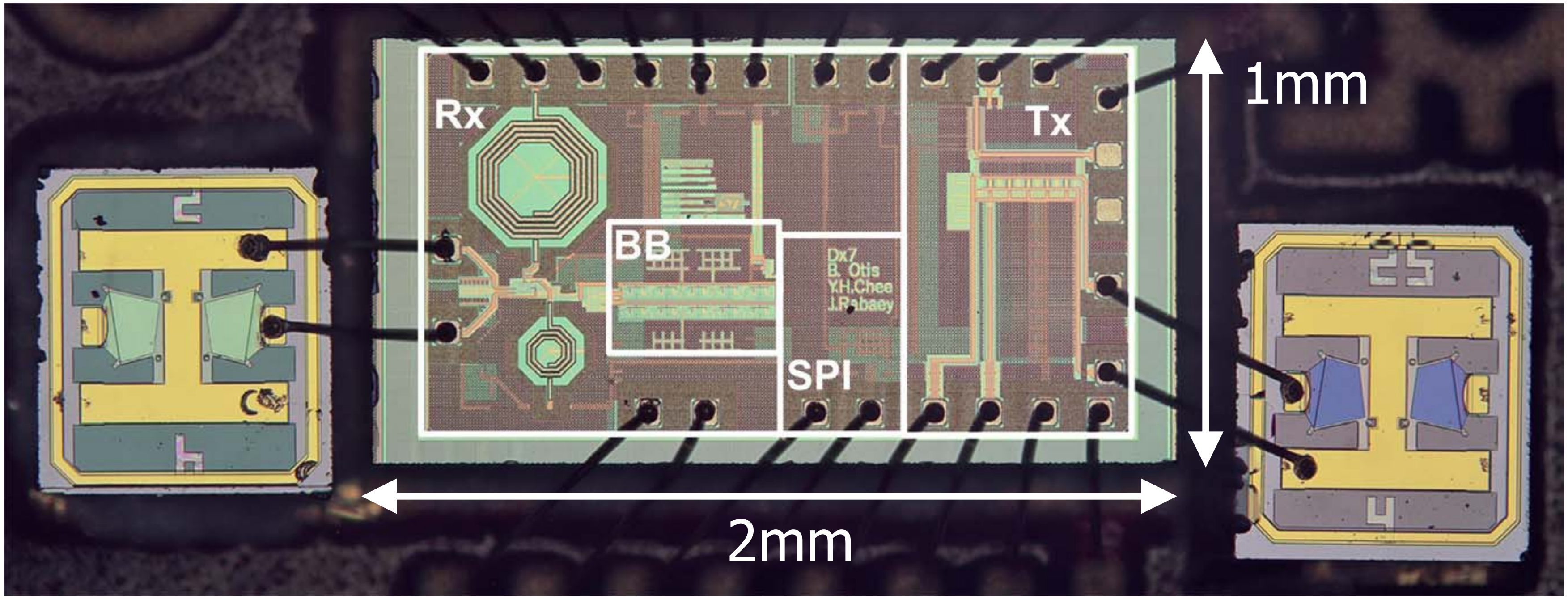
Transmit Beacon

2004 (Pletcher / Otis)



Passive receiver

Fully Integrated 1mm^3 Rx/Tx



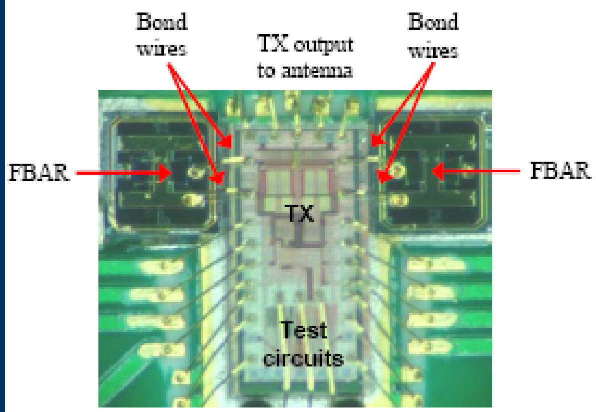
- No external components (inductors, crystals, capacitors)
- 400µW from 1V in 0.13µm CMOS
- Very small implementation volume

Presented at ISSCC 2005

B. Otis, Y.H. Chee

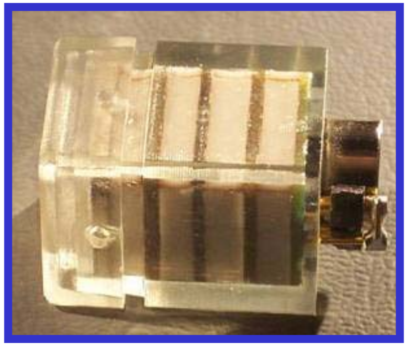
(More) Radio History in the Group

Active Antenna Transmitter



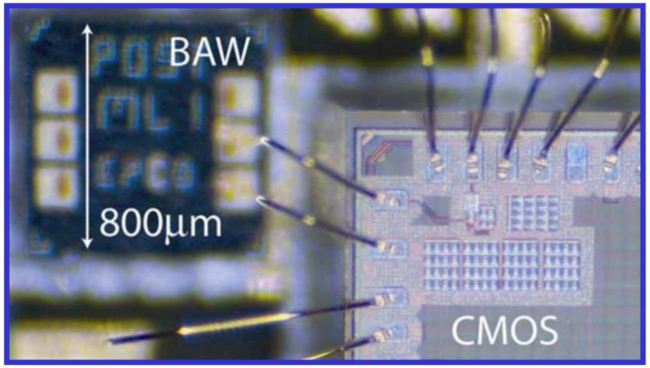
VLSI 2006 (Chee)

PicoCube



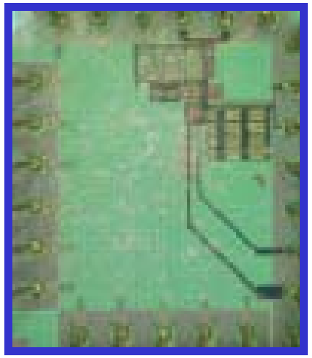
2006 (Burghardt et al)

Wakeup Receiver



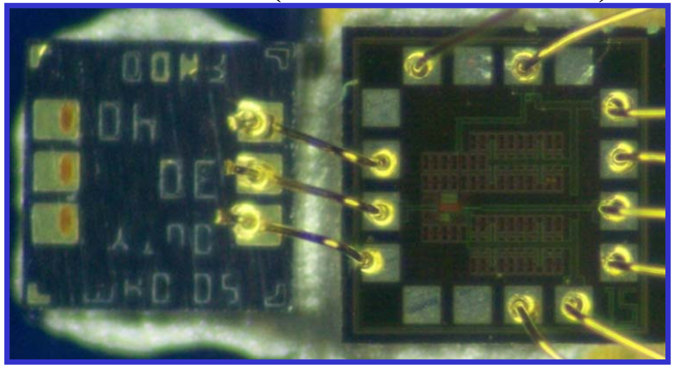
2008 (Pletcher)

JSSCC 2006 (Chee)



Injection Locked Transmitter

2007 (Mark/Richmond)



Temperature compensation

Reducing Power Even Further

Key Characteristics of DR Networks:

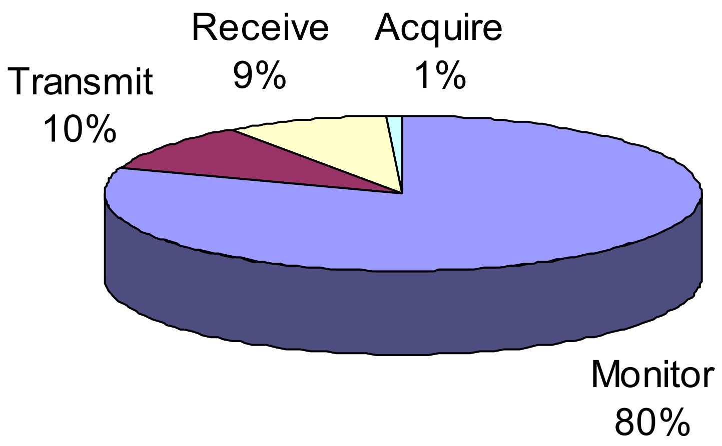
- Low packet traffic rates
- Short packets (< 200 bits)

Monitor power dominant:

- Reduce monitor power through heavy duty-cycling
- Need to solve the problem of synchronization between motes

Time spent in different states for a CSMA/CA MAC protocol

(802.11 @ 10 packets/sec)

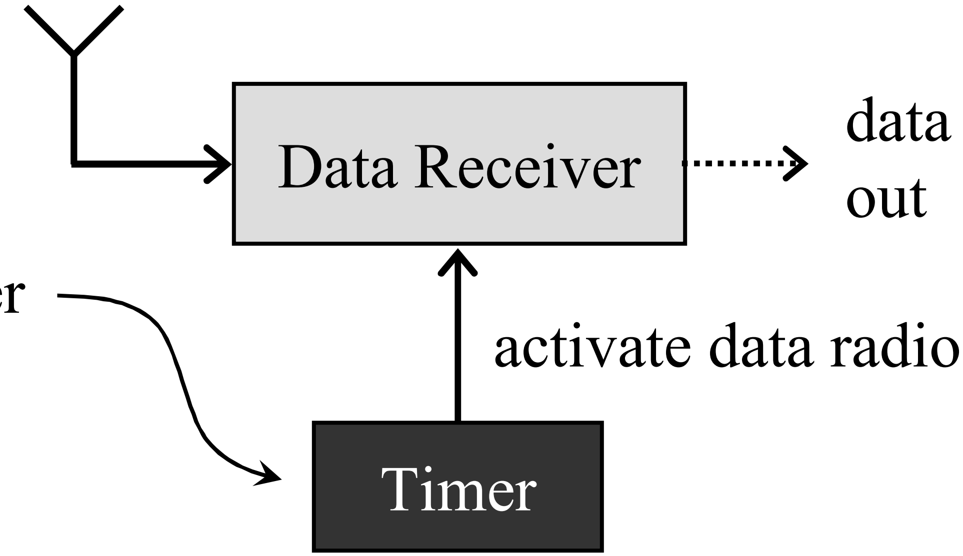


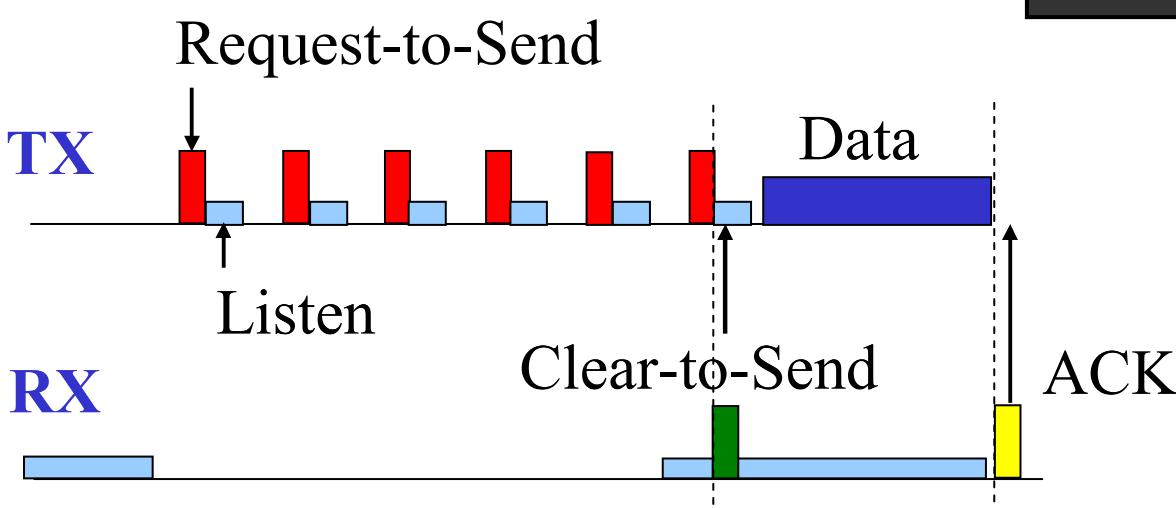
Adapted from: Lin Ph.D. 2005

Exploiting Low Duty-Cycles

Protocol-Based Duty-Cycling

Timer duty-cycles receiver

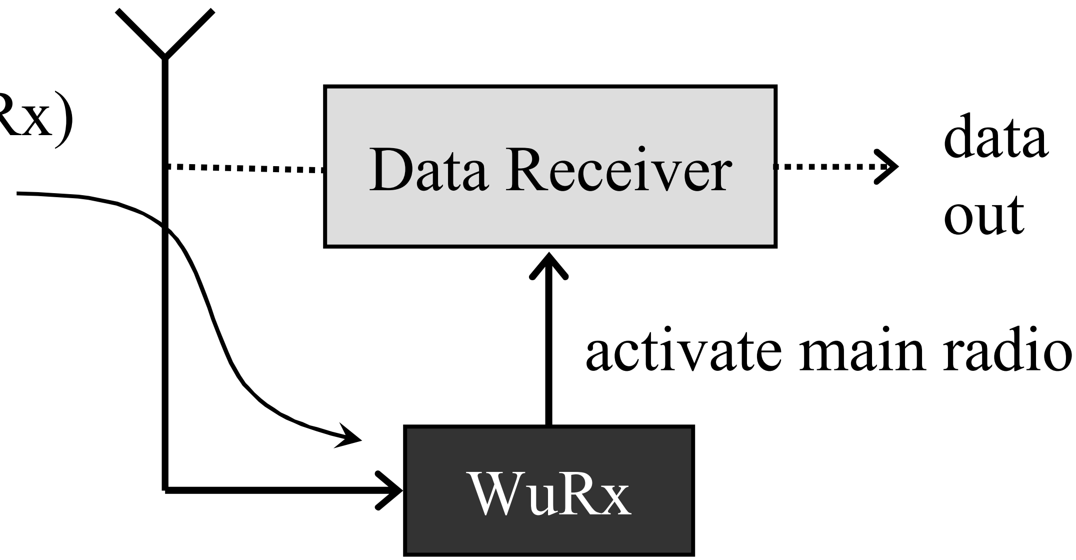


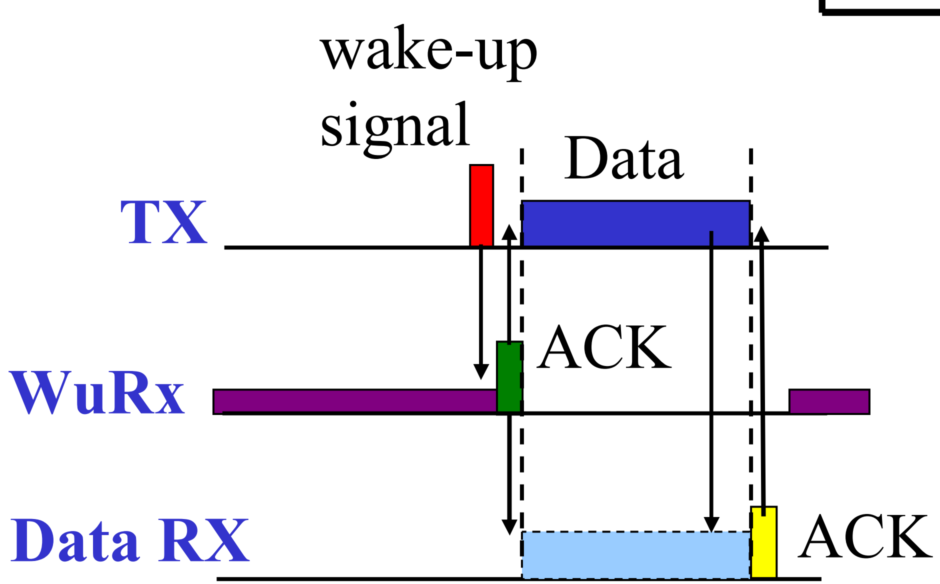


Trade-off between network latency and average power

Duty-Cycling with Wake-up

Wake-up receiver (WuRx) listens for requests and controls duty-cycle

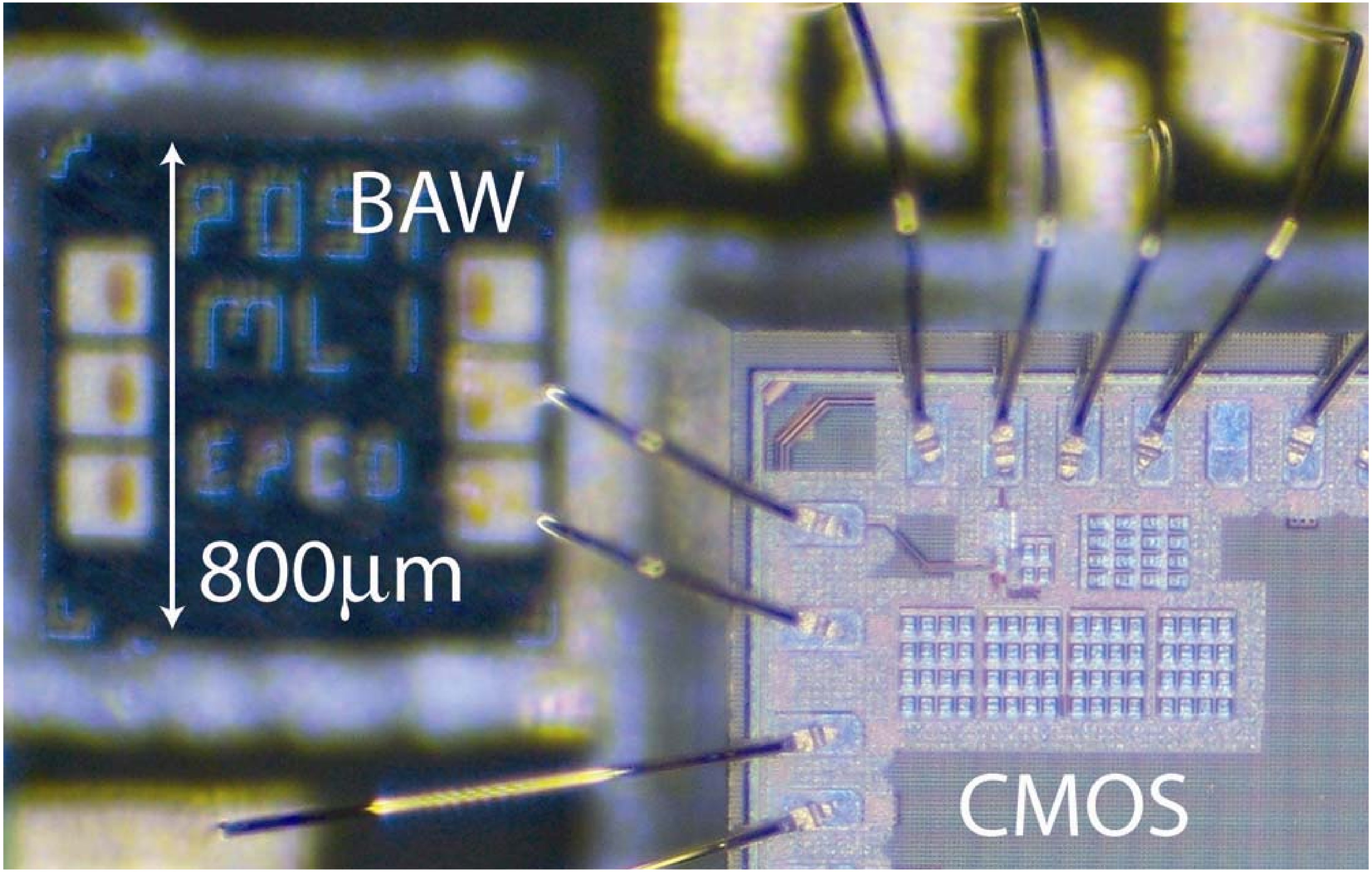




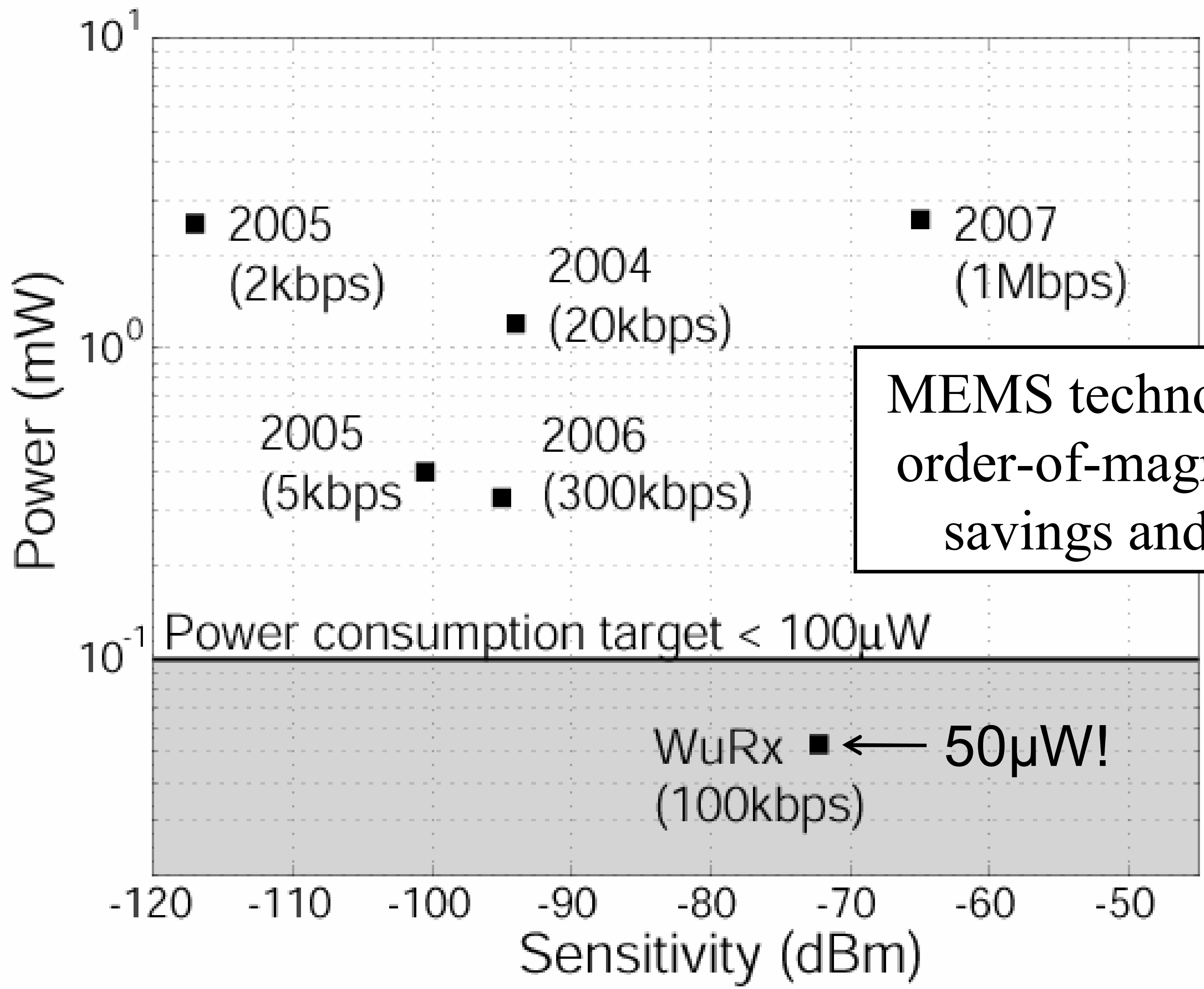
- Reduces network latency
- Requires ultra-low power (<100µW)

Prototype Wake-up Receiver

90nm standard digital CMOS



Reaching the Power Target



MEMS technology enables order-of-magnitude power savings and small size

Micro-Power/Cost Wireless

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